EMC Compliance Procedure
For Electrical/Electronic
Components and Subsystems

Foreword

The modern automobile represents an extremely harsh electromagnetic environment. Full compliance with this procedure will help ensure electromagnetic compatibility (EMC) between all electrical and electronic components located within the vehicle and between each component and the external electromagnetic environment of the vehicle.

This procedure relates to all active electronic modules and sensors (i.e. incorporating IC's and transistors), motors, generators, solenoids and passive modules.

Date	Version	Written/Revised	Revision
30/11/13	1	A Martin	First Release
16/12/13	1.1	M Beetlestone	ESD guidance added to section 2 Test Plan Guide.
13/05/15	1.2	M Beetlestone	DV results added to section 1, retest selection added to section 4. eTracker date changed from PTCC to IDJ. Upper and under body timing combined. Note on HV component test plan added to section 2.
19/08/15	1.3	M Beetlestone	Flow chart updated to include AIMS process

Table of Contents:

1. EMC Component Compliance.

The flow chart shown in Fig 1 provides an overview of the component EMC process, a more detailed description is as follows:

New Components

When a new component is identified the details necessary for the EMC database are provided by the electronic submission of the component information via the EMC eTracker found at:
www.etracker.jlr.ford.com/default.asp?ProjectID=EMCTRACK this is completed by the responsible component engineer prior to <IDJ>.

If the part already exists on the eTracker, i.e. carry over from a previous platform, the new programme will be added to the eTracker. If the part is modified using the Management of Change process then a new eTracker must be raised. If the part is significantly different to the original part or has different operating modes then a new eTracker and test plan will be required.

Component EMC Test Plan

The Supplier must provide a test plan for each component or sub-system applicable for EMC testing. JLR EMC must approve the test plan prior to test commencement.

A guide for producing a Test plan is shown in **Section 3**.

The test plan shall be submitted no later than 60 days prior to **FDJ**.

When a test plan is agreed the test plan front sheet will be signed by the JLR EMC engineer, component owner and the Supplier. The eTracker status will then be changed to No Test Results.

Component EMC Test Facility

The EMC test facility shall be one approved by JLR EMC and the process for this approval is detailed on the website www.jaguarlandrover.com/emc

The JLR EMC engineer may accept test data at their discretion from a test facility during the period between applying for and receiving final approval. This decision will be influenced by any National or International accreditation or approval already held by the test facility (e.g. UKAS in the UK) and whether or not a test facility report, as described in JLR-EMC-CS has been submitted.

Component EMC Test Results

Test reports shall comply with the requirements of ISO 17025.

All test reports shall include a reference to the approved Test Plan or Management of Change tracking number and include sign-off by the laboratory verifying the test results

All test reports shall consist of a single PDF document and contain a summary page at the beginning, which shows the compliance status of each test.
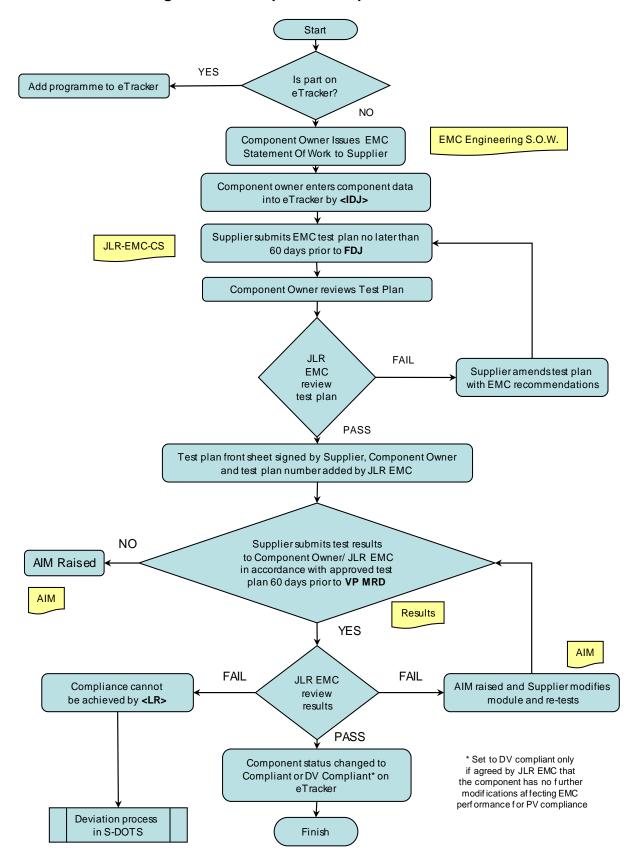
Test results must be submitted to JLR EMC o later than 60 days prior to **VP MRD**.If the results comply with all the requirements of JLR-EMC-CS and have been obtained in accordance with the procedures and test methods described in the approved component test plan then JLR EMC may approve the results. The results are attached to the eTracker and the part marked as DV compliant for Design Validation results or Compliant for Product Verification results.

If the results of one or more tests fail the requirements of JLR-EMC-CS, then the supplier is expected to resolve the issue and re-test the module in accordance with the approved test plan and re-submit test results. **If compliance cannot be achieved by the appropriate gateway then the component engineer will be responsible for raising a deviation in accordance with the JLR deviation Procedure in S-DOTS.**

Fig 1.0 EMC Component Compliance Flowchart

```
                              Start

          YES
Add programme to eTracker  ◄──── Is part on eTracker?

                              NO

            Component Owner Issues EMC          EMC Engineering S.O.W.
            Statement Of Work to Supplier

            Component owner enters component data
            into eTracker by <IDJ>

JLR-EMC-CS   Supplier submits EMC test plan no later than
             60 days prior to FDJ

            Component Owner reviews Test Plan

                JLR              FAIL        Supplier amends test plan
                EMC            ─────────►     with EMC recommendations
                review
                test plan

                PASS

            Test plan front sheet signed by Supplier, Component Owner
            and test plan number added by JLR EMC

         NO        Supplier submits test results
AIM Raised ◄────    to Component Owner/ JLR EMC
                    in accordance with approved test
AIM                 plan 60 days prior to VP MRD    Results

                              YES                                    AIM

Compliance cannot   FAIL    JLR EMC    FAIL    AIM raised and Supplier modifies
be achieved by <LR> ◄────   review    ────►    module and re-tests
                            results

                              PASS           * Set to DV compliant only
                                               if agreed by JLR EMC that
            Component status changed to         the component has no further
            Compliant or DV Compliant* on       modifications affecting EMC
            eTracker                            performance for PV compliance

Deviation process
in S-DOTS                     Finish
```

2. Test Plan Guide

In general the completed test plan should be a self-contained document i.e. it should not reference other design specifications. The plan should be sufficiently detailed to provide an EMC test technician, who is not familiar with the product, with all the necessary information to perform testing and evaluate the results for all tests listed in the plan.

The Test Selection Matrix is contained in the EMC standard JLR-EMC-CS in table 6.1.

For a component with many variants then separate test plans must be produced for each variant and different test plan numbers will be allocated. Where the variants are simply left and right e.g. lights then a single plan will suffice and a single report will be issued but high and low line headlamps would require separate plan.

For Hybrid and Electric Vehicle components a special template is available from the JLR EMC Engineers along with a document called *Guidance on EMC for High Voltage DC components.*

3. Description of the Test Plan Sections

Product Name

The name of the component or module must match that used in the eTracker.

Product Supplier Name

Provide manufacturers name and address, indicate first and second tier supplier where applicable.

Approved EMC Test Facility

Indicate test facility(s) to be used. **The lab must be approved by JLR following the process detailed on the website** www.jaguarlandrover.com/emc   Test results from non-approved labs cannot be used and will be rejected.

Product part number(s)

JLR part numbers are required for all DUT's covered by the testing in this plan. If the DUT is only supplied as part of a larger assembly then the assembly part number can be given.

Vehicle and Model Year

List **all programs and model years** where part(s) covered in this plan are used.

EMC Specification Used

Show which EMC test specification will be adhered to during test set-up and testing e.g. JLR-EMC-CS v1.0.

Superseded specifications cannot be used.

Test Plan Revision History

Test Plan Revision History

Date	Supplier Reference	Description	Approved Issue No
08-08-13	v0.1	Initial draft	
09-08-13	v0.2	Update as per JLR EMC review comments	1
10-08-13	v0.3	Revised plan for JLR specification change	
11-08-13	v0.4	Update as per JLR EMC review comments	2

For Internal EMC Department Use		
Test Plan Tracking Number	JLR-EMC-201X-XXXX	Issue No. 2

Supplier Reference

The working reference to be updated (by the supplier) during the test plan review process (actual format is not important).

Approved Issue No.

A record of the document version previously approved by all parties. This is be completed by the JLR EMC engineer when the plan is approved.

Issue No.

The Issue number of the approved test plan.

Filenames

The test plan is then saved by the EMC engineer, as last approver, with the file naming convention as follows:-

"JLR-EMC-201X-XXXX Issue 2.pdf"

The document name is then "JLR-EMC-201X-XXXX Issue 2" when uploaded to the eTracker

NB: Any additional MOCs are titled - **"JLR-EMC-201X-XXXX-A.pdf"** The MOC document itself will then reference the corresponding test plan (and issue number) which is to be used for testing.

Surrogate Data forms will be labelled **"JLR-EMC-201X-XXXX-SD.pdf"** In the unusual situation where there is more than one SD form then the suffix will become **SD2**. The test report will then reference the Test Plan number and the Surrogate Data number.

Introduction

This section provides JLR with general information about the Device under test (DUT) to be submitted for test.

Product Family Description

DUT may be part of a family of related devices such as those on earlier or other programs. If so provide similarities and differences between them, systems diagrams including power and control signals may be helpful for this purpose. The information provided here may help to justify test sample surrogate selection (see section 2.3 of the template). For example an electro-chromatic interior rear view mirror may be one of a family of three: Electrochromatic only, electrochromatic with compass and electrochromatic with compass and automatic head lamp control.

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Theory of Operation

Provide a description of the DUT operation, suitable for those not familiar with the product. **Avoid references to other specifications** (which the reader may not have easy access to).

- What does the DUT do?
- How and when does it operate?
- **Include a block schematic diagram that shows the connections to the vehicle, particularly the power supply**.

Physical Construction

General information regarding module/PCB construction. e.g. housing material, number of connectors, PCB material and number of layers. **It is particularly important to show connector diagrams with pin location and assignment details. Add a picture of the DUT and include its major dimensions.**

Vehicle Packaging

Where is the component located and how is it connected to ground.

EMC Requirements Analysis

This section provides an understanding of which circuits are likely to be a risk in terms of susceptibility or emissions. Obviously those signals or circuits where operation is critical ought to be a priority for monitoring during immunity testing and likewise during emissions tests it is important that those circuits likely to cause high emissions are active.

Critical Interface Signals

Signals listed here are potentially susceptible or critical to correct operation. This may be all of the signals or just a few, but must include power and ground; otherwise the DUT will not operate.

Potential Sources of Emissions

Circuits or signals, which are a possible emissions risk. i.e. PWM signals, oscillators, high frequency circuits, data signals, high current or voltage signals, inductive or capacitive switching etc.

Test Sample / Surrogate selection

It may be acceptable to test a single part variant **(remember two samples minimum!)** to represent all other variants in a family of related devices. Test results from this part will then provide surrogate data for the other parts. This will obviously reduce the cost and effort required and will therefore be an attractive route for achieving component EMC compliance. **However technical justification will be required**. For example it may be acceptable to only test the most comprehensive variant of a range of Electrochromatic mirrors. Justification for doing so would be necessary, as an example it may be the case that all mirrors in the family have the same PCB layout with identical housing construction and materials the only difference being minor component population differences.

Test Design and Requirements.

This is the core of the test plan including DUT Modes and Functions, test requirements and input/output requirements for each test.

DUT Operating Modes/Functional Classifications

This section is often completed incorrectly so please read the following carefully;

This section essentially provides a master reference for all DUT 'Modes' and 'Functions' names that appear throughout the rest of the plan. **All Mode and Functions listed in the plan must be classified and defined in this section; this ensures consistency and avoids any misunderstandings**. **The JLR Product Development Component Owner(s) and their supplier(s) shall be responsible for developing these classifications and performance requirements.**

Table 3.1 is where the overall DUT functionality is broken down into 'Modes' and 'Functions'. Think of a 'Mode' as the state that the DUT or system is in and a 'Function' as something that is capable of being performed in that particular 'Mode'. Examples of modes could be 'ON', 'OFF' and 'Standby'. Several 'Functions' may be active in any given 'Mode'. Examples of 'Function' names are:- 'Purge valve opened', 'Ignition', 'CAN communications', 'LED illumination', 'PWM motor drive active', 'Read ADC' etc..

The possible 'Functions' for each of the modes listed shall be classified as either Class A (convenience), B (enhance vehicle operation and control) or C (essential to vehicle operation and control) by entering the function names under the appropriate column of table 3.1. (For full functional importance classification definitions see Section 3.0 in JLR-EMC-CS).

An 'X' shall be placed in the appropriate 'Vehicle Operating Modes' column to indicate in what vehicle mode the DUT Functions can be active.

Finally 'Mode' and 'Function' definitions shall be described in a manner suitable for those not familiar with the product i.e. what each mode and function is or does.

A simplified example of the modes and functions that might be available for an instrument cluster is shown below;

DUT Mode	DUT Functions			Vehicle Operating Modes			
	Class A	Class B	Class C	Off	Accessory	Start	Run
Operating		Vehicle speed			X		X
		Warning lamps			X		X
	Message centre				X		X
Standby		Fuel level					X
	Ambient Temperature				X		X

Note: modes and functions listed above are for illustration only and not necessarily correct for a real instrument cluster.

Mode Description(s):

Operating – cluster is fully operational providing speed, rev counter and warning lamp information

Standby – cluster is in standby mode with ignition in accessory position, providing fuel level and temperature readings.

Function Description(s):
Vehicle speed – the cluster is decoding CAN messages provided by the braking system and displaying a reading of the current vehicle speed on the speedometer, etc.

Test Requirements

This section lists which tests are applicable to the DUT and what Modes and Functions will be activated and monitored for each test. **This table shall only contain the modes and function names already defined in section 3.1 to avoid confusion.**

A "Y" or "N" shall be placed in the "Test Applies" column to indicate whether or not the test listed in the table is applicable. See section 6.0 of the component EMC specification, JLR-EMC-CS for help assessing the applicability of each EMC test.

The "Interface to be tested" column shall be used to indicate which circuits the test applies to and whether or not multiple interfaces/circuits shall be tested combined or separately - denoted by placing a "C" or "S" after the interface name.

Finally, the last column shall include which Modes or Functions (listed in section 3.1) are to be activated during each applicable test, but shouldn't include details of the actual tests.

Test Description	Test applies (Y/N)	Functional Class & Functional Status			Interface to be tested	S/C[1]	Operating Mode(s) to be used for indicated test
		A	B	C			
Radiated Immunity – RF							
RI 112 Level 2 BCI	Y	II	II	I	All circuits	C	

Note: it may not be feasible or practical to operate all available modes and functions listed in table 3.1 for each test. However in the case of immunity tests all Class C modes must be exercised. During emissions testing the Modes/Functions likely to cause the worst case emissions shall be active.

A technical justification is required for any test marked as not applicable.

Input Requirements

Sufficient information shall be included here for a technician who is not familiar with the product to be able to configure the DUT in the Modes/Functions necessary for each test. This may be in the form of electrical inputs (e.g. Batt, GND, Control signals, CAN messages etc) to be entered in the table provided or other non electrical inputs such as a sequence of key presses or other mechanical inputs.

For each operating mode chosen in section 3.2, list all the input signals that are required to place the DUT in the required operating mode in the table provided. List the EMC tests to which the mode applies in the "Test" column. **State the connector pin numbers to which the signals are applied and include details of waveform, amplitude, frequency, pulse width, duty cycle and any other details necessary to accurately produce the signal required.**

Output Requirements

This section shall be used to define what electrical signals or other indicators will be used to monitor and verify correct operation of each mode and function being activated during each test. Electrical parameters shall be listed in the table provided. For non-electrical indicators the format is free provided that "Nominal" (N) and "Acceptance criteria" (A) parameters are provided. Examples of non-electrical indicators are position, rpm, pressure, brightness etc.

Note: if the electrical signals to be monitored apply to all tests then "All" can be written in the "Test" column to indicate this rather than listing all tests names separately **– please do not leave blank**. The table may be split or expanded to cover each function or test separately if this helps to simplify the table.

For each parameter to be monitored, the Nominal parameter (N) and Acceptance criteria (A) together, define what is essentially the functional performance status I (i.e. operate as designed). Additional definitions for functional performance status II must also be included to define the minimum acceptable performance should any deviation from designed performance be observed during exposure. See Section 3.0 of JLR-EMC-CS for a full definition.

The acceptance criteria parameter (A) shall be chosen such that the allowable deviation is equal to the upper limit where the degradation in functionality becomes perceivable to the customer.

The Status I performance is not applicable to every test or function; in each test section of the EMC component specification the expected performance status (I, II or III) appropriate to each Functional Importance Classification (A, B or C) is provided - see section 3.0 of EMC specification for full definition of importance classifications.

Note: it is not necessary to define the conditions required to meet performance status II or III performance criteria since by definition, deviating outside the limits defined for the status I criteria means by default that the function will be operating to either a class II (if recovery on removal of test condition is automatic) or class III (if recovery requires operator intervention) performance status. Conditions for Class I, II and III performance status are fully defined in Section 3.0 in JLR-EMC-CS.

For emissions tests use this section to state what parameters, in the form N ±A, are monitored to verify that the DUT is functioning representatively, for the duration of the emissions frequency sweep. e.g. use the current drawn by a dc motor to verify that it is operating at the correct torque, motor RPM could be monitored by using an optical or magnetic sensors positioned close to the motor's shaft.

In the case of the time domain emissions test, use this section to state the parameters to monitor just before the switching event. i.e. for a solenoid or motor state the nominal (N) operating current together with the allowable deviation (A). This is an important check since the current disconnected will have a significant effect on the voltage transient measured, $V= -Ldi/dt$.

For ESD an example is given below

CI 280 ESD Parametric Value Requirements

Parameter Name	Nominal Value	Tolerance	Reason for change within tolerance band	Reason for change out of tolerance band	Notes
e.g. LIN pin leakage current	0uA	±1uA	Measurement uncertainty at low current	ESD damage to an interface component (LIN IC, capacitor, or suppressor	Due to capacitance on the line, allow time for measurement to stabilise.

Load Box/Test Support Requirements

This section is used to describe the requirements for the load box/test fixture. The test fixture is necessary to provide the input stimulus and output loadings necessary to represent as near as practical the actual vehicle installation e.g. **all output drive circuits within the load box should be representative of the real drive circuits used on the vehicle and all load values should also be representative in terms of resistance, capacitance and inductance.**

Details of the test fixture shall be entered in the table provided. Information including DUT pin numbers, names, and descriptions and whether each pin is an input or output must be entered. If a pin is loaded, indicate by placing an 'X' in the appropriate column, whether it is connected to a real or simulated termination. Information on additional support hardware/software requirements should be included where applicable. Note: where possible the content of the load box/test fixture should be passive so as not to influence the test performance.

A test fixture diagram may be used in place of the table provided sufficient detail is provided on the electrical loading applied to each input and output pin of the DUT.

DUT Test Set-up

The information presented in this section shall permit reproduction of the same test set-up by another test laboratory.

It is recognised that approved test facilities are capable of component/sub-system setup within the test environments shown in the EMC specification JLR-EMC-CS.
The approved test facility shall provide details of the setup as part of the formal test report.
Specific test exceptions / differences to these test requirements shall be documented in this section.
Standard setup sheets have been provided for convenience and may be used to document this information.
ESD test points shall be included even if there is no deviation from the specified test method.

4.   Process for Repeat EMC Testing

Changes to the component's original production design may often impact its EMC characteristics. Often some EMC testing needs to be repeated to verify there is no negative impact. Information provided in this annex presents a process for assessing what EMC testing shall be required when specific component design changes are being considered.

Information provided in Table 4.0 shall be used by the Component Owner and the Supplier to determine what EMC tests shall be required to validate the design changes. The Supplier shall notify the owner of the component and the JLR EMC department prior to commencement of testing. The component's original EMC test plan shall be used to facilitate the testing. Deviations from this process shall be pre-approved by the JLR EMC department.

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Table 4.0   Retest requirements

* Modification Type	Change	Requirement Applies (✓)																
		RE 310	CE 420	CE 410	RI 112	RI 114	RI 115	RE 320	RI 140	RI 130	RI 150	CI 210	CI 220	CI 230	CI 250	CI 265	CI 270	CI 280
Component Changes	I/O Capacitor	✓	✓		✓	✓	✓											✓
	Regulator Capacitor (I/P)	✓	✓		✓	✓	✓						✓	✓	✓			
	IC decoupling Capacitor	✓	✓															
	Slew Rate Capacitors	✓	✓		✓	✓	✓											
	Op Amp Input Capacitors				✓	✓	✓											
	I/O Series Resistors	✓	✓		✓	✓	✓											✓
	Slew Rate Resistors	✓	✓		✓	✓	✓											
	Zener or MOV on Battery												✓				✓	
	Microprocesor	✓	✓		✓	✓	✓											
	Oscillator	✓	✓											✓				
	PWM Controler	✓	✓															
	Change of memory	✓	✓		✓	✓	✓			✓	✓							✓
	Change of regulator supply level	✓	✓	✓	✓	✓	✓			✓	✓	✓	✓	✓	✓	✓	✓	✓
	Change of supply filtering	✓	✓	✓	✓	✓	✓			✓	✓	✓	✓	✓	✓	✓	✓	✓
	PCB components depopulation/population	✓	✓	✓	✓	✓	✓			✓	✓							✓
	LIN/CAN/Flexray interfaces changes	✓	✓		✓	✓	✓			✓	✓							✓
Software Changes	PLL Frequency	✓	✓		✓	✓	✓											
	O/P Slew Rate (Increase or Decrease)	✓	✓	✓														
	Watchdog, Reset, Intrerupt				✓	✓	✓			✓	✓							
	Change of PWM	✓	✓		✓	✓	✓											
	Change of signal repetition rate	✓	✓		✓	✓	✓											
PCB / Electrical Interconnect	I/O to external connection	✓	✓		✓	✓	✓											✓
	MUX Lines (e.g. SCP, CAN)	✓	✓															
	Reset Lines				✓	✓	✓			✓	✓							
	Low Level Analog				✓	✓	✓			✓	✓							
	Ground Plane	✓	✓		✓	✓	✓			✓	✓							✓
	Change to board layers	✓	✓															
	Supply Lines / High Currents	✓	✓		✓	✓	✓											
	PCB Rerouting, change of technology	✓	✓		✓	✓	✓											✓

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* Modification Type	Change	Requirement Applies (✓)																
		RE 310	CE 420	CE 410	RI 112	RI 114	RI 115	RE 320	RI 140	RI 130	RI 150	CI 210	CI 220	CI 230	CI 250	CI 265	CI 270	CI 280
Packing and/or Mechanical Changes	Packing Material	✓	✓		✓	✓	✓											✓
	Grounding	✓	✓		✓	✓	✓											✓
	Heatsink	✓	✓															✓
	Apertures																	✓
	Change of geometry																	✓
Loading changes	Solenoids, Motors, Relays			✓														
	Active Sensors				✓	✓	✓								✓			
Manufacturing	Manufacturing Relocation	✓	✓		✓	✓	✓											✓
	Change of process	✓	✓		✓	✓	✓											✓

* NOTE: This matrix is not an exhaustive list. The test list is defined by the supplier in MoC and aproved by the JLR EMC engineer prior to any testing.

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5.   Management of Change for EMC

The purpose of this section is to give guidance to suppliers for assessing the impact of design changes on electromagnetic compatibility and choosing appropriate tests to repeat. The website www.jaguarlandrover.com/emc contains a template, which must be completed and submitted to the relevant responsible JLR Component Engineer and then the EMC team for approval.

Evaluating the exact impact of a change on the final EMC performance requires an in depth understanding of both electronic and electromagnetic characteristic of the module. Sometimes, this may require back-to-back testing. The Supplier engineers, designers and the EMC experts, are best placed to analyse the change and decide which EMC tests to repeat. At JLR, we expect to be advised by the supplier as to what is being changed, the analysis of the expected impact on EMC characteristics and what tests shall be repeated. We will review the supplier's analysis and any supporting data used for selecting which tests to repeat, if any. The JLR EMC team reserved the right to request additional tests based on the information provided. It is however the responsibility of the supplier to ensure that their components remain compliant and that proof of this compliance can be demonstrated at a later date if required.

Selecting EMC tests to repeat after a change:

All previously applicable tests shall be performed unless technical reasoning is provided and agreed as to why the changes will not impact on the results of that test.

All tests shall be performed in an approved facility to JLR-EMC-CS at its latest issue.

6.   Requirements for "off the shelf" components

The purpose of this section is to give guidance to component owners and suppliers for assessing the impact of introducing "off the shelf" components on electromagnetic compatibility and choosing the appropriate additional tests to perform.

A test plan must be submitted and approved in accordance with section 1 of this document along with a completed EMC Component Testing Surrogate Data Submission Form. The website www.jaguarlandrover.com/emc contains a template, which must be completed and submitted to the relevant responsible JLR Component Engineer and then the JLR EMC team for approval.

Assessing data from tests performed to other EMC specifications against the JLR EMC specification requires an in depth understanding of the test specifications applied. Sometimes, this may require additional testing. It is recommended that the test laboratory that performed the original testing is requested to perform such comparison as they are best placed to analyse the data and decide which EMC tests to repeat or perform. If a different laboratory is requested to perform the Surrogate Data analysis then they must be approved by JLR and the process for approval is shown on the JLR website. JLR will review the analysis and any supporting data used for selecting which tests to perform. The JLR EMC team reserves the right to request additional tests based on the information provided. It is however the responsibility of the supplier to ensure that their components remain compliant and that proof of this compliance can be demonstrated at a later date if required.

Selecting EMC tests to perform when introducing "off the shelf" components:

All applicable tests shall be performed unless technical reasoning is provided and agreed as to why it will not impact on the results of that test, or surrogate data is provided which demonstrates the JLR EMC requirements have been met or exceeded.

All tests shall be performed in an approved facility to JLR-EMC-CS at its latest issue.

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